

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate; and

a bonding pad portion formed on said semiconductor substrate, said

5 bonding pad portion comprising:

an insulating film formed on said semiconductor substrate and a

first-level conductive pad layer of a large island shape formed on said insulating film;

first-level to (n-1)-level (n is an integer of 3 or larger) interlayer insulating films formed on and over said insulating film;

10 second-level to n-level conductive pad layers formed on said interlayer insulating films in areas generally corresponding to an area where said first conductive pad layer was formed;

a plurality of small diameter first through holes from the first-level to (n-1) level formed through said first-level to (n-1) level interlayer insulating films in
15 areas generally corresponding to an area where said first conductive pad layer;

a plurality of first contact plugs filled in said small diameter first through holes from the first-level to (n-1)-level, said first contact plugs at each level being conductive and electrically connecting two conductive pad layers adjacent along a normal to a surface of said semiconductor substrate, among said first-level to n-level
20 conductive pad layers disposed in and on said first-level to (n-1)-level interlayer insulating films;

an n-level interlayer insulating film formed on said (n-1)-level interlayer insulating film and covering said n-level conductive pad;

a large diameter through hole formed through said n-level interlayer
25 insulating film in an area corresponding to an area where said n-level conductive pad was formed, said large diameter through hole having a size corresponding to said

n-level conductive pad to expose a substantial upper surface of said n-level conductive pad; and

a bonding pad formed on said n-level interlayer insulating film and n-level conductive pad via said large diameter through hole.

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2. A semiconductor device according to claim 1, further comprising a wiring portion comprising:

first-level to n-level wiring layers formed on and over said semiconductor substrate at same levels as said first-level to n-level conductive pad layers;

a highest-level wiring layer formed on said n-level interlayer insulating film;

small diameter second through holes formed through said first-level to n-level interlayer insulating films; and

a plurality of second contact plugs filled in said small diameter second through hole from the first-level to n-level, said second contact plug at each level being conductive and electrically connecting two wiring layers adjacent along a normal to the surface of said semiconductor substrate, among said first-level to n-level wiring layers disposed in and on said first-level to n-level interlayer insulating films.

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3. A semiconductor device according to claim 2, further comprising wiring patterns for connecting said bonding pad layer and said wiring layer at a same-level.

4. A semiconductor device according to claim 3, wherein said interlayer insulating film includes a coated insulating film.

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5. A semiconductor device according to claim 4, wherein said bonding pad portion is formed around said wiring portion.

6. A semiconductor device according to claim 4, wherein said conductive pad layer includes a Ti layer, an Al-Cu alloy layer and a TiN layer.

7. A semiconductor device according to claim 4, wherein said conductive pad layer includes an Al-Cu alloy layer and a TiN layer.

8. A semiconductor device according to claim 4, wherein a diameter of said small diameter first through hole is two times or smaller than a diameter of said small diameter second through hole.

9. A semiconductor device according to claim 4, wherein said first and second contact plugs are made of W.

10. A semiconductor device according to claim 4, wherein said first and second contact plugs each comprise:

a first layer of Ti, Ti/TiN or TiN covering an inner surface of each of said small diameter first and second through holes; and
W layer formed thereon.

11. A semiconductor device according to claim 4, wherein said interlayer insulating film contains silicon oxide.

12. A semiconductor device according to claim 4, wherein a silicon oxide

film and a silicon nitride film are formed on said n-level interlayer insulating film.

13. A method of manufacturing a semiconductor device, comprising the steps of:

- 5 (a) forming an insulating film on a semiconductor substrate;
- (b) forming first conductive pads of a large island shape on the insulating film;
- (c) forming a first interlayer insulating film on the insulating film, the first interlayer insulating film covering the first conductive pad layer;
- 10 (d) forming a second conductive pad layer on the first interlayer insulating film in an area corresponding to the first conductive pad layer;
- (e) forming a small diameter first through hole through the first interlayer insulating film in an area corresponding to an area where the first conductive pad layer was formed;
- 15 (f) filling a conductive first contact plug in the small diameter first contact hole to electrically connecting the first and second conductive pad layers;
- (g) sequentially repeating said steps (c) to (f) to form second-level to n-level (n is an integer of 3 or larger) conductive pad layers and second-level to (n-1)-level interlayer insulating films and electrically connect two conductive pad
- 20 layers adjacent along a normal to a surface of the semiconductor substrate;
- (h) forming an n-level interlayer insulating film on the (n-1)-level interlayer insulating film;
- (i) forming a large diameter through hole through the n-level interlayer insulating film, the large diameter through hole having generally a same size as the
- 25 n-level conductive pad layer; and
- (j) forming a bonding pad on the n-level interlayer insulating film, the

bonding pad being electrically connected to the n-level conductive pad layer via the large diameter through hole.

14. A method of manufacturing a semiconductor device according to claim

5 13, further comprising a step of:

(h) forming a passivation film on the n-level interlayer insulating film, the passivation film exposing the bonding pad, after said step (j).

15. A method of manufacturing a semiconductor device according to claim

10 14, wherein said step (h) forms a silicon oxide film and a silicon nitride film.

16. A method of manufacturing a semiconductor device according to claim

13, wherein said step (c) of forming the first interlayer insulating film comprises the steps of:

15 forming a silicon oxide film;

coating hydrogen silsesquioxane resin on the silicon oxide film;

thermally treating the hydrogen silsesquioxane to form a first ceramic silicon oxide film; and

forming a thick silicon oxide film on the first silicon oxide film by plasma

20 CVD.

17. A method of manufacturing a semiconductor device according to claim

16, further comprising a step of planarizing the second silicon oxide film by CMP.

25 18. A method of manufacturing a semiconductor device according to claim

16, further comprising a step of planarizing the second silicon oxide film by etching.

19. A method of manufacturing a semiconductor device according to claim 13, wherein said step (f) comprises the steps of:

forming a Ti interlayer insulating film covering an inner surface of the small diameter first through hole;

5 forming a TiN layer on the Ti interlayer insulating film; and
forming a W layer on the TiN layer.

20. A method of manufacturing a semiconductor device according to claim 13, wherein said step (f) comprises the steps of:

10 forming a Ti interlayer insulating film covering an inner surface of the small diameter first through hole by sputtering;

forming a TiN layer on the Ti interlayer insulating film by sputtering; and
forming a W layer on the TiN layer.

15 21. A method of manufacturing a semiconductor device according to claim 13, wherein said step (f) comprises the steps of:

forming a Ti interlayer insulating film covering an inner surface of the small diameter first through hole;

forming a TiN layer on the Ti interlayer insulating film; and

20 forming a W layer on the TiN layer by blanket CVD.

22. A method of manufacturing a semiconductor device according to claim 13, wherein said step of forming the conductive pad layer comprises the steps of:

forming a Ti layer;

25 forming an Al-Cu alloy layer;

forming a Ti layer; and

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The diagram illustrates the proposed system architecture. It features a central 'Proposed System' block, which is connected to 'User' and 'System' blocks. The 'Proposed System' block is further divided into 'User' and 'System' sub-blocks. The 'User' sub-block is connected to 'User' and 'System' blocks. The 'System' sub-block is connected to 'User' and 'System' blocks. The 'Proposed System' block is also connected to 'User' and 'System' blocks. The 'Proposed System' block is also connected to 'User' and 'System' blocks.